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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,126	10/24/2003	Edward B. Stokes	GLOZ 2 00170	1739
27885	7590	09/22/2005		
FAY, SHARPE, FAGAN, MINNICH & MCKEE, LLP 1100 SUPERIOR AVENUE, SEVENTH FLOOR CLEVELAND, OH 44114			EXAMINER IM, JUNGHWA M	
			ART UNIT	PAPER NUMBER
			2811	
DATE MAILED: 09/22/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/693,126	<b>Applicant(s)</b> STOKES ET AL.	
	<b>Examiner</b> Junghwa M. Im	<b>Art Unit</b> 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 2-18, 29 and 30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2-13, 16, 17, 29 and 30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 14, 15 and 18 are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7/11/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-8, 10-12, 16-17 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Camras et al. (US 6784463), hereinafter Camras in view of Sawayama et al. (US 6788366), hereinafter Sawayama.

Regarding claim 3, Fig. 3A of Camras shows a flip chip light emitting diode die [100] including:

a light-transmissive substrate [117; col.4, lines 64-66];

a plurality of semiconductor layers [114, 112, 116, 124] disposed on the light-transmissive substrate, the semiconductor layers including a p-type layer and an n-type layer [col. 4, lines 28-33], the semiconductor layers defining a device mesa; and

a reflective electrode [118; a reflective contact] disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa, the reflective electrode including electrical connecting material [118a; col. 6, lines 10- 29] disposed over portions of the device mesa and making electrical contact with the device mesa, the reflective electrode having laterally periodic reflectivity modulations (through having a waveform of reflectivity in terms of time). Fig. 3A of Camras shows most aspect of the instant invention except "a light-transmissive

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dielectric layer laterally interspersed with the electrical connecting material.” Fig. 4 of Sawayama shows a reflective electrode [14] wherein a light-transmissive dielectric layer [5c] laterally interspersed with the electrical connecting material [12].

It would have been obvious to one ordinary skilled in the art at the time of the invention made to incorporate the teachings of Sawayama into the device of Camras in order to have the a light-transmissive dielectric layer laterally interspersed with the electrical connecting material to protect the reflective electrode.

Regarding claim 2, it is obvious that the periodic reflectivity modulations in Fig. 3A of Camras define a diffraction grating that provides a predetermined diffraction of the light produced by the device mesa since a diffraction grating is realized through the reflective electrode having a laterally periodic modulation.

Regarding claim 4, the combined structure resulting from Fig. 3A of Camras and the dielectric layer of Sawayama shows the electrical connecting material [118a] defines isolated regions, and an electrically conductive reflective layer [118c] disposed over the dielectric layer and the electrical connecting material, the reflective layer laterally electrical interconnecting the isolated regions of the electrical connecting material.

Regarding claim 5, Fig. 4 of Camras shows an electrically conductive bondable layer [132; a solder layer] disposed on the electrically conductive reflective layer.

Regarding claim 6, Fig. 3 of Camras shows a current-spreading layer [124] disposed between the device mesa and the dielectric layer.

Regarding claim 7, Fig. 3 of Camras shows the current-spreading layer includes a light-trans missive electrically conductive layer (col. 7, lines 8-24).

Regarding claim 8, even though Camras discloses that the light-transmissive electrically conductive layer includes a thin film of light-absorbing material (through being a distributed Bragg reflector; col. 7, lines 16-19), the combined teachings of Camras and Sawayama fail to show that “the thin film having a thickness of less than about 10 nm and greater than 70% light transmission.” However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have “the thin film having a thickness of less than about 10 nm and greater than 70% light transmission” in order to improve the light transmission, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 10, Camras discloses that the current-spreading layer includes a topmost one or more of the plurality of semiconductor layers (through forming a part of a distributed Bragg reflector; col. 7, lines 16-19)

Regarding claim 11, it is obvious that the dielectric layer incorporated to the device of Camras with the teachings of Sawayama has a thickness selected to define an interference reflector optimized for a characteristic wavelength of the light produced by the device mesa as a practice for routine optimization.

Regarding claim 12, the combined teachings of Camras and Sawayama does not explicitly show that “the interspersing of the electrical connecting material and the dielectric layer define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa.” However, it is obvious that the device with the combined teachings of Camras and Sawayama has the characteristics in which the interspersing of the

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electrical connecting material and the dielectric layer define a reflection diffraction grating optimized for a characteristic wavelength of the light produced by the device mesa since the waveform of the reflectivity is realized by the interspersing of the electrical connecting material and the dielectric layer.

Regarding claim 16, Fig. 7E of Camras shows an interface disposed between the plurality of semiconductor layers and the reflective electrode is roughened to scatter the reflected light toward the sides of the device mesa (col. 13, lines 5-7).

Regarding claim 17, Fig. 7E of Camras shows roughening therefore, it is obvious that the device with combined teachings of Camras and Sawayama would include a lateral periodicity defining a diffraction grating through having a waveform in terms of time (col. 13, lines 1-10 of Camras).

Regarding claim 29, Fig. 3A of Camras shows a flip chip light emitting diode die [100] including:

a light-transmissive substrate [117; col.4, lines 64-66];

a plurality of semiconductor layers [114, 112, 116, 124] disposed on the light-transmissive substrate, the semiconductor layers including a p-type layer and an n-type layer [col. 4, lines 28-33], the semiconductor layers defining a device mesa; and

a reflective electrode [118; a reflective contact] disposed on the device mesa to energize the device mesa to produce light and to reflect the light produced by the device mesa toward at least one of the light-transmissive substrate and sides of the device mesa, the reflective electrode including electrical connecting material portions [118a; col. 6, lines 10- 29] disposed over the device mesa and making electrical contact with the device mesa. Fig. 3A of Camras shows most

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aspect of the instant invention except “a light-transmissive dielectric layer laterally interspersed with the electrical connecting material.” Fig. 4 of Sawayama shows a reflective electrode [14] wherein a light-transmissive dielectric layer [5c] laterally interspersed with the electrical connecting material [12].

It would have been obvious to one ordinary skilled in the art at the time of the invention made to incorporate the teachings of Sawayama into the device of Camras in order to have the a light-transmissive dielectric layer laterally interspersed with the electrical connecting material to protect the reflective electrode.

Regarding claim 30, Fig. 3A of Camras shows the electrical connecting material portions are isolated from one another and the combined teachings of Camras and Sawayama show the reflective electrode further includes: an electrically conductive reflective area [118c; reflective metal] disposed over the connecting material portion and the dielectric portions, the reflective layer laterally electrical interconnecting the isolated electrical connecting material portions.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Camras and Sawayama as applied to claim 8 above, and further in view of Ramdani et al. (US 5838707), hereinafter Ramdani.

Regarding claim 9, the combined teachings of Camras and Sawayama show most aspect of the instant invention except “the light-absorbing material is selected from a group consisting of nickel oxide, gold, indium tin oxide, and zinc oxide.” Fig. 3 of Ramdani shows a reflective electrode [36; a distributed Bragg reflector] having a the light-absorbing material is selected

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from a group consisting of nickel oxide, gold, indium tin oxide, and zinc oxide (col. 5, lines 28-35).

It would have been obvious to one ordinary skilled in the art at the time of the invention made to incorporate the teachings of Ramdani into the device of Camras and Sawayama in order to have the light-absorbing material selected from a group consisting of nickel oxide, gold, indium tin oxide, and zinc oxide for a better reflectivity.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Camras and Sawayama as applied to claim 3 above, and further in view of Chua et al. (US 5838707), hereinafter Chua.

Regarding claim 13, the combined teachings of Camras and Sawayama show most aspect of the instant invention except “the dielectric layer is selected from a group consisting of a silicon oxide, a silicon nitride, and a silicon oxynitride.” Chua discloses a dielectric material formed in a reflective electrode [142 in Fig. 3; a distributed Bragg reflector] selected from a group consisting of a silicon oxide, a silicon nitride, and a silicon oxynitride(col. 7, lines 1-3).

It would have been obvious to one ordinary skilled in the art at the time of the invention made to incorporate the teachings of Chua into the device of Camras and Sawayama in order to have the dielectric layer is selected from a group consisting of a silicon oxide, a silicon nitride, and a silicon oxynitride since these dielectric materials are well known in the industry.

***Allowable Subject Matter***

Claims 14-15 and 18 are allowed.



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The following is an examiner's statement of reasons for allowance.

Prior art fails to teach or render obvious a semiconductor device with combinations of elements as set forth in the claims, including in particular a flip chip light emitting diode with the topmost one or more of the plurality of semiconductor layers of the dielectric layer including first portions having a first refractive index, and further including second semiconducting portions laterally interspersed amongst the first portions and having a second refractive index different from the first refractive index, the first portions and the second semiconducting portions cooperatively defining the topmost one or more of the plurality of semiconductor layers.

And additionally, Prior art fails to teach or render obvious a semiconductor device with combinations of elements as set forth in the claims, including in particular a flip chip light emitting diode with an insulating grid having openings at which the electrical connecting material is disposed and a reflective layer over the insulating grid and the electrical connecting material and electrically interconnecting the electrical connecting material at the openings wherein the roughened interface is an interface between the reflective layer and the insulating grid.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

Applicant's arguments filed June 30, 2005 have been fully considered but they are not persuasive.

Applicant argues that "First, Sawayama relates to a LCD display, not to a semiconductor device. The layer (30) is a scattering-type liquid crystal (see at least col. 8 lines 46-47). This is non-analogous art, and would not be referenced by the skilled artisan to develop a new design for a reflective electrode for a semiconductor." It is pointed out that Sawayama relates to an LCD which include a semiconductor device (4). Therefore, the Sawayama reference is analogous art since it is within the field of the inventor's endeavor.

Applicant argues that "Second, Applicants find no indication that the dielectric layer (5c) is light-transmissive, as called for in claim 3. Indeed, there is no need in Sawayama for dielectric layer (5c) to be light-transmissive. The dielectric layer (5c) provides a corner cube array (10) morphology for the multiple reflective electrodes (12) formed of reflective metallic layers disposed on the dielectric layer (5c). The reflective electrodes (12) are opaque (the reflective metal layers have thicknesses of 100nm or higher). See Sawayama col. 8 line 40 through col. 9 line 1. Most of the dielectric film (5c) is covered by the opaque metal layers of the reflective electrodes (12), so that the light does not reach the dielectric film (5c)." It is pointed out that the dielectric layer of the instant invention is made of the material which is well known and commonly used for inter-level dielectrics. And these well-known and commonly used inter-level dielectrics are light-transmissive since they are not completely light-reflective or completely light-absorbing. Furthermore, it is pointed out that the instant invention discloses that the reflective layer (46) of the reflective electrode (34) is made of opaque silver or silver/titanium.

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Therefore, most of the dielectric film of the instant invention is also covered by the opaque metal layers.

Finally, Applicant argues that “Nothing in either Camras or Sawayama would suggest to the skilled artisan this motivation, or any other motivation, for interspersing a light-transmissive dielectric layer with electrical connecting material in a reflective electrode for a semiconductor.” Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 189 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 595 (CCPA) 1969.

### *Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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